Dynamic Models of Multilevel Converters by using the Power Oriented Graph Technique

Roberto Zanasi and Stefania Cuoghi

***Abstract*—The advances in power electronics, and new needs in renewable energy sources lead the multilevel converters to be advantageous compared to 2-level converters. Since modeling tools can be helpful to design new converter topology, this paper presents the dynamic models of the three basic topologies of multilevel converters: the Diode-Clamped, the Flying-Capacitor and the Cascaded H-Bridge converters. These models have been obtained by using the Power Oriented Graph (POG) technique, that is easy to be employed and implemented in Matlab-Simulink® environment. The proposed models are suitable to simulate high frequency sliding mode control and can be easily modified to model hybrid topologies. Simulation results confirm the validity of the presented models.**

***Index Terms*—Modeling technique, multilevel converters, power control.**

I. Introduction

In recent years, the research interest on multilevel converters has been increasing, leading to a rapid development of new topologies and control strategies, [1]-[4]. In particular, the advances in power electronics and new emerging needs in renewable energy systems and smart grid applications make the use of multilevel converters a promising alternative to classical 2-level converters, [5]-[6]. The main advantages are related to low total harmonic distortion (THD), low voltage stress of power switching devices and a namely low reduction of voltage derivative, reducing the filter dimension and increasing the system efficiency and power conversion, [7]-[8]. For these characteristics the multilevel converters are particularly interesting for high power applications. Moreover they are suitable for Photovoltaic (PV) systems, since the modularity of the PV arrays provides different DC voltage levels as direct sources of the converter, see [9].

In this continuously evolving scenario, modeling tools can be helpful to manufactures to reduce the time and the cost of the design of new topologies and control strategies. However the libraries of commercial tools are not always updated to the recent architectures. Moreover the high frequency of the PWM control signals make many of these tools inadequate to the simulation. In this paper the dynamic model of some basic multilevel converter topologies obtained by using the so called Power Oriented Graph (POG) modeling technique will be presented. This technique was introduced in 1991, see [10]-[12], and it is based on the same energetic approach firstly introduced by H.M. Paynter in 1960 and used in the Bond Graph technique. One of the main advantage of the POG technique is its easy implementation in Matlab-Simulink® environment. In power electronic contest, the POG technique has been employed to model a grid connected photovoltaic system, see [13]-[15]. In particular the POG models of a dual active-bridge DC/DC converter and a single phase H-Bridge DC/AC converter have been introduced and simulated. In this paper the POG models of multilevel converters will introduced for the first time. In particular, the dynamic models of three basic kinds of multilevel topologies will be presented: the Diode-Clamped topology [16], the Flying-Capacitor topology [17]-[18] and the Cascaded H-Bridge topology [19]-[20]. The state-space equations of these topologies can be easily obtained by the models and used to design new control strategies.

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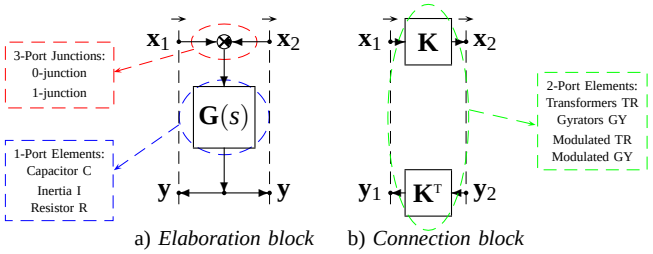

a) *Elaboration block* b) *Connection block*

Fig. 1. POG basic blocks: *elaboration block* and *connection block*.

Simulation results have been obtained in Matlab-Simulink® environment by using three types of PWM modulation algorithms: the Phase Disposition PWM (PD-PWM), the Phase Opposition Disposition PWM (POD-PWM) and the Alternate Phase Opposition Disposition PWM (APOD-PWM) algorithms, [9].

The paper is organized as follows. In Sec. II the Power Oriented Graphs modeling technique is presented. In Sec. III, IV and V the models of Diode-Clamped, Flying-Capacitor and Cascaded H-Bridge topologies are presented. Simulations results and conclusions end the paper.

II. The Power-Oriented Graphs (POG) technique

The POG is a graphical modeling technique based on the same energetic approach of the Bound Graph (BG) technique, but it uses a different graphical notation. The two POG basic blocks are the elaboration block and the connection block, see Fig. 1. The first is used for modeling all the physical elements that can store and/or dissipate energy, while the second is used for modeling all the physical elements that transform the power without losses. The elaboration block corresponds to the 1-port element in BG technique (capacitor, inertia,

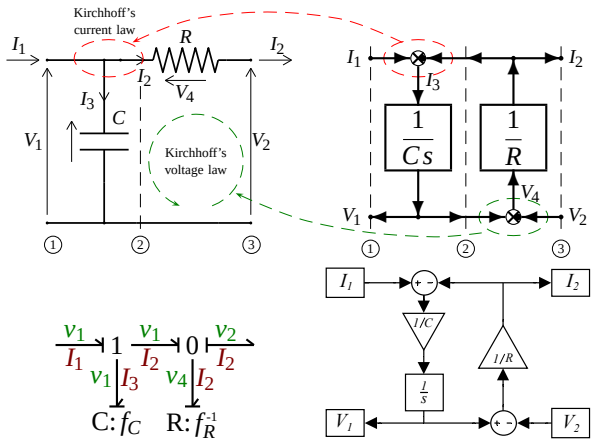

Fig. 2. Electrical circuit of CR filter, corresponding POG model, BG model and Matlab/Simulink® scheme.

resistor), while the sum element at the top of the elaboration block corresponds to the 3-port BG connection elements (0-junctions or 1-junctions). The connection block denotes all the 2-port elements of the BG technique: transformer, gyrators, modulated transformer and modulated gyrators. The dashed lines in Fig. 1 denote the power sections which connect the POG blocks to the external world. The scalar product $\mathbf{x}^T\mathbf{y}$ of the two *power vectors* $\mathbf{x}$ and $\mathbf{y}$ involved in each dashed line of a POG scheme, have the physical meaning of *the power flowing through that particular section*, see Fig. 1.

Let us consider the simple electrical example of the CR filter shown in Fig. 2. The corresponding POG model is shown on the top right, while the BG model is shown on the bottom left of the figure. Both the techniques provide the exact mathematical model of the system. While the BG scheme is quite compact, the POG model is easy to use, easy to understand and can be directly implemented in Matlab-Simulink® environment, see the block scheme on the bottom right of Fig. 2.

III. POG model of Diode-Clamped converter

First in this section the POG model of a 3-level Diode-Clamped or Neutral Point Clamped (NPC) converter will be described and then this model will be extended to n-level NPC converters.

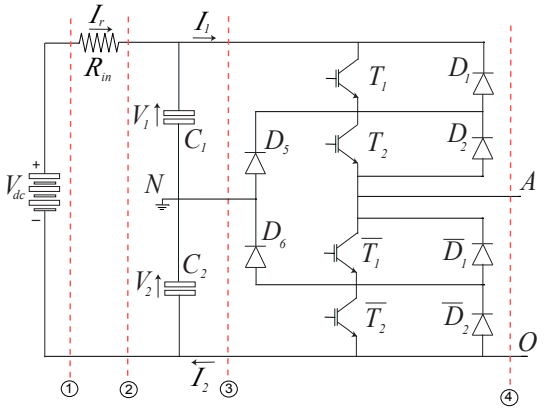

Fig. 3. Three-level Diode-Clamped converter scheme.

T_1	T_2	$\overline{T_1}$	$\overline{T_2}$	V_{AN}	V_{AO}
1	1	0	0	$V_{dc}/2$	V_{dc}
0	1	1	0	0	$V_{dc}/2$
0	0	1	1	$-V_{dc}/2$	0

TABLE I
Control signals T_i and output voltages V_{AN} and V_{AO} in the case of 3-level Diode-Clamped converter.

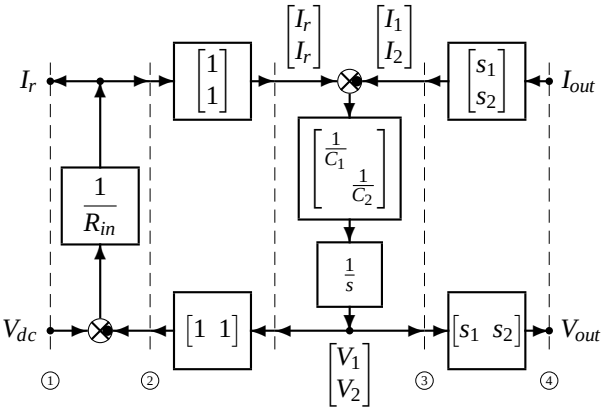

Fig. 4. POG model of 3-level Diode-Clamped Converter.

The classical electrical scheme of 3-level Diode-Clamped converter is shown in Fig. 3, while the corresponding POG dynamic model is given in Fig. 4. The first block present between sections ① and ② describes the model of the input resistance R_{in}. The connection and elaboration blocks present between sections ② and ③ represent the model of the input capacitors C_1 and C_2, those dynamical equations can be written as

$$V_1 = \frac{1}{C_1 s}(I_r - I_1), \qquad V_2 = \frac{1}{C_2 s}(I_r - I_2).$$

Referring to sections ③ and ④ of Fig. 3, let $T_i = \{T_1, T_2, \overline{T_1}, \overline{T_2}\}$ denote the control signals of the transistors. The state $0/1$ of T_i denotes the state OFF/ON of the corresponding transistor. The waveforms of T_i are generated by the control system such to connect C_1 and/or C_2 to the output. The three-levels of output voltages V_{AO} and V_{AN} are shown in Tab. I and their control can be obtained by different PWM modulation techniques, see [9]. The corresponding POG model is represented by the connection blocks between the corresponding sections in Fig. 4. In particular, the switching control signals s_1 and s_2 have been determined neglecting the dissipative losses of the converter and by using the relations between signals T_i and the output voltages $V_{out} = V_{AO}$ and $V_{out} = V_{AN}$ described as follows

$$\begin{aligned} V_{AO} &= \begin{bmatrix} T_1 & T_2 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} s_1 & s_2 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}, \\ V_{AN} &= \begin{bmatrix} T_1 & \overline{T_2} \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix} = \begin{bmatrix} s_1 & s_2 \end{bmatrix} \begin{bmatrix} V_1 \\ V_2 \end{bmatrix}. \end{aligned} \tag{1}$$

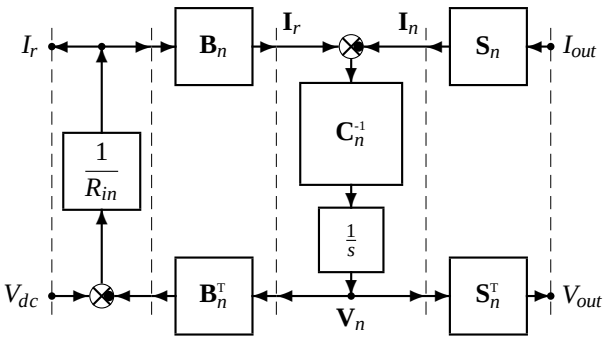

Fig. 5. POG model of m-level Diode-Clamped and Flying-Capacitor converters.

T_1	T_2	T_3	T_4	V_{AN}	V_{AO}
1	1	1	1	$V_{dc}/2$	V_{dc}
0	1	1	1	$V_{dc}/4$	$3V_{dc}/4$
0	0	1	1	0	$V_{dc}/2$
0	0	0	0	$-V_{dc}/4$	$V_{dc}/4$
0	0	0	0	$-V_{dc}/2$	0

TABLE II
CONTROL SIGNALS T_i AND OUTPUT VOLTAGES IN THE CASE OF A 5-LEVEL DIODE-CLAMPED CONVERTER.

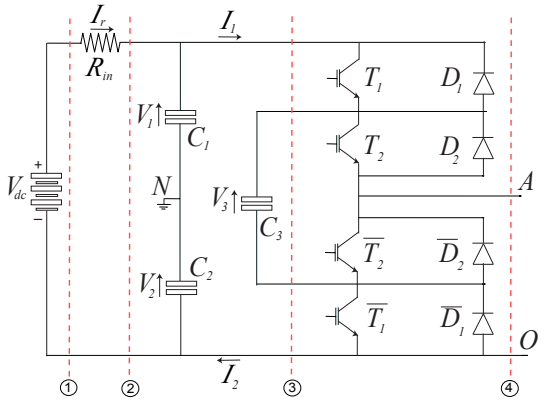

Fig. 6. Electrical scheme of 3-level Flying-Capacitor converter.

T_1	T_2	$\overline{T_1}$	$\overline{T_2}$	V_{AN}	V_{AO}
1	1	0	0	$V_{dc}/2$	V_{dc}
1	0	0	1	0	$V_{dc}/2$
0	1	1	0	0	$V_{dc}/2$
0	0	1	1	$-V_{dc}/2$	0

TABLE III
CONTROL SIGNALS T_i AND OUTPUT VOLTAGES IN THE CASE OF 3-LEVEL FLYING-CAPACITOR CONVERTER.

The state-space equations of the converter are the following

$$\begin{bmatrix} C_1 & 0 \\ 0 & C_2 \end{bmatrix}\begin{bmatrix} \dot{V}_1 \\ \dot{V}_2 \end{bmatrix}=\begin{bmatrix} -\frac{1}{R_{in}} & 0 \\ 0 & -\frac{1}{R_{in}} \end{bmatrix}\begin{bmatrix} V_1 \\ V_2 \end{bmatrix}-\begin{bmatrix} s_1 \\ s_2 \end{bmatrix} I_{out}+\begin{bmatrix} \frac{1}{R_{in}} \\ \frac{1}{R_{in}} \end{bmatrix} V_{dc}. \quad (2)$$

The extension of the POG model to m-level NPC converter is shown in Fig. 5, where vectors $\mathbf{B}_n$, $\mathbf{S}_n$ and matrix $\mathbf{C}_n$ are defined as follows

$$\mathbf{B}_n=\begin{bmatrix} 1 \\ 1 \\ \vdots \\ 1 \end{bmatrix}, \quad \mathbf{S}_n=\begin{bmatrix} s_1 \\ s_2 \\ \vdots \\ s_n \end{bmatrix}, \quad \mathbf{C}_n=\begin{bmatrix} C_1 & & & \\ & C_2 & & \\ & & \ddots & \\ & & & C_n \end{bmatrix},$$

where $n=m-1$. In particular the vector $\mathbf{S}_n$ is a function of the desired output voltage V_{out}

$$\begin{cases} \mathbf{S}_n=[T_1,T_2,...,T_n]^{\mathrm{T}} & \text{if} \quad V_{out}=V_{AO}, \\ \mathbf{S}_n=[T_1,...,T_{\frac{n}{2}},-\overline{T_{\frac{n}{2}+1}},...,-\overline{T_n}]^{\mathrm{T}} & \text{if} \quad V_{out}=V_{AN}. \end{cases}$$

In the case of a 5-level converter the relationships between control signals T_i and the output voltages V_{AO} and V_{AN} are shown in Tab. II. In this case it is $\mathbf{S}_n=[T_1,T_2,T_3,T_4]$ when $V_{out}=V_{AO}$ and $\mathbf{S}_n=[T_1,T_2,-\overline{T_3},-\overline{T_4}]$ when $V_{out}=V_{AN}$.

IV. POG MODEL OF FLYING-CAPACITOR CONVERTER

The electrical scheme of a 3-level Flying-Capacitor converter is shown in Fig. 6. The relations between the admissible configurations of control signals T_i and the corresponding values of the output voltages V_{AN} and V_{A0} are shown in Tab. III. The corresponding POG model is shown in Fig. 7, where $\mathbf{C}_m$ is a diagonal matrix with the values of capacitors C_1,C_2,C_3 in its diagonal. The switching signals s_1,s_2,s_3 can be obtained by the input-output relationships shown in Tab. III as follows

$$\begin{cases} [s_1,\ s_2,\ s_3]=[T_1,\ T_1,\ \overline{T_1}T_2-T_1\overline{T_2}] & \text{if} \quad V_{out}=V_{AO} \\ [s_1,\ s_2,\ s_3]=[T_1,\ -\overline{T_1},\ \overline{T_1}T_2-T_1\overline{T_2}] & \text{if} \quad V_{out}=V_{AN} \end{cases}$$

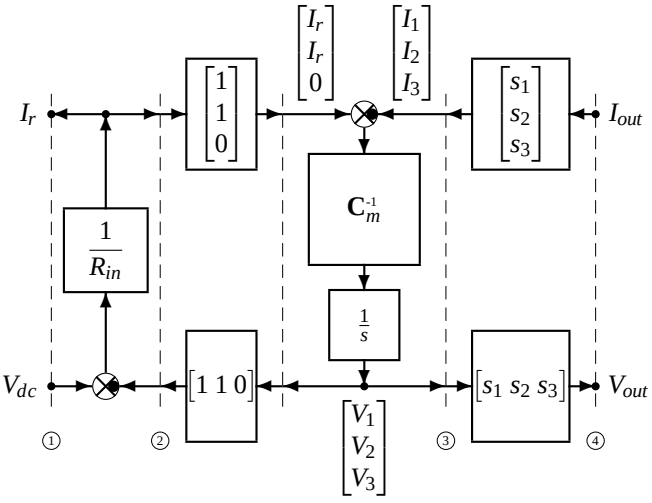

Fig. 7. POG model of a 3-level Flying-Capacitor converter.

The state-space equations of 3-level Flying-Capacitor converter are the following

$$\begin{bmatrix} C_1 & 0 & 0 \\ 0 & C_2 & 0 \\ 0 & 0 & C_3 \end{bmatrix}\begin{bmatrix} \dot{V}_1 \\ \dot{V}_2 \\ \dot{V}_3 \end{bmatrix}=\begin{bmatrix} -\frac{1}{R_{in}} & 0 & 0 \\ 0 & -\frac{1}{R_{in}} & 0 \\ 0 & 0 & 0 \end{bmatrix}\begin{bmatrix} V_1 \\ V_2 \\ V_2 \end{bmatrix}-\begin{bmatrix} s_1 \\ s_2 \\ s_3 \end{bmatrix} I_{out}+\begin{bmatrix} \frac{1}{R_{in}} \\ \frac{1}{R_{in}} \\ 0 \end{bmatrix} V_{dc}. \quad (3)$$

The POG model of the Flying-Capacitor converter generalized to the m-level case is still represented by the POG scheme

shown in Fig. 5. In this case it is $n=m$, $\mathbf{B}_n=[1\,1\,0\,0\,0\,...]^{\mathrm{T}}$, while $\mathbf{C}_n$ is a m-dimensional diagonal matrix characterized by the values of the equivalent capacities of each branch of the circuit. The state space equations of the converter are the following

$$\left[\begin{array}{cc|ccc} C_1 & 0 & 0 & \dots & 0 \\ 0 & C_2 & 0 & \dots & 0 \\ \hline 0 & 0 & C_3 & \dots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & \dots & C_n \end{array}\right]\left[\begin{array}{c} \dot{V}_1 \\ \dot{V}_2 \\ \hline \dot{V}_3 \\ \vdots \\ \dot{V}_n \end{array}\right]=\left[\begin{array}{cc|ccc} -\frac{1}{R_{in}} & 0 & 0 & \dots & 0 \\ 0 & -\frac{1}{R_{in}} & 0 & \dots & 0 \\ \hline 0 & 0 & 0 & \dots & 0 \\ \vdots & \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & 0 & \dots & 0 \end{array}\right]\left[\begin{array}{c} V_1 \\ V_2 \\ \hline V_3 \\ \vdots \\ V_n \end{array}\right]-\left[\begin{array}{c} S_1 \\ S_2 \\ \hline S_3 \\ \vdots \\ S_n \end{array}\right]I_{out}$$

$$+\left[\begin{array}{c} \frac{1}{R_{in}} \\ \frac{1}{R_{in}} \\ \hline 0 \\ \vdots \\ 0 \end{array}\right]V_{dc}, \qquad I_r=-\left[\begin{array}{cc|ccc} \frac{1}{R_{in}} & \frac{1}{R_{in}} & 0 & \dots & 0 \end{array}\right]\left[\begin{array}{c} V_1 \\ V_2 \\ \hline V_3 \\ \vdots \\ V_m \end{array}\right]+\frac{1}{R_{in}}V_{dc}.$$

In the case of a 5-level converter the control signals s_i have the following expression

$$[s_1,s_2,s_3,s_4,s_5]=[T_1,T_1,\overline{T_1}T_2-T_1\overline{T_2},\overline{T_2}T_3-T_2\overline{T_3},\overline{T_3}T_4-T_3\overline{T_4}]$$

when $V_{out}=V_{AO}$ and the expression

$$[s_1,s_2,s_3,s_4,s_5]=[T_1,\overline{T_1},\overline{T_1}T_2-T_1\overline{T_2},\overline{T_2}T_3-T_2\overline{T_3},\overline{T_3}T_4-T_3\overline{T_4}]$$

when $V_{out}=V_{AN}$.

V. POG model of Cascaded H-Bridge converter

A 3-level Cascaded H-Bridge converter is a single H-Bridge converter represented in Fig. 8. The relationships between control signals T_i and the output voltage $V_{out}=V_{AO}$ are described in Tab. IV, the corresponding POG model is shown in Fig. 9. It can be easily shown that in this case the switching control signal is $s_1=\overline{T_2}T_1-T_2\overline{T_1}$.

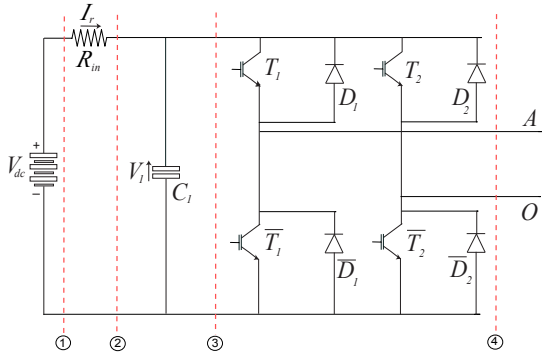

Fig. 8. Electrical scheme of 3-level Cascaded H-Bridge converter.

T_1	T_2	$\overline{T_1}$	$\overline{T_2}$	V_{AO}
1	0	0	1	V_{dc}
1	1	1	0	0
0	0	1	1	0
0	1	1	0	$-V_{dc}$

TABLE IV
Control signals T_i and output voltage V_{AO} in the case of 3-level Cascaded H-Bridge converter.

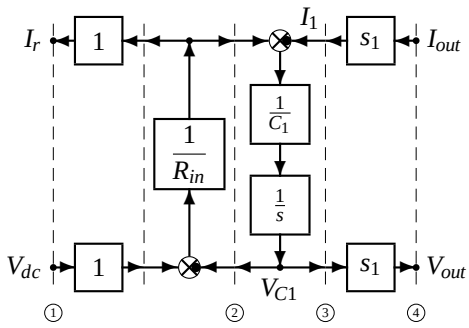

Fig. 9. POG dynamic model of a 3-level Cascaded H-Bridge converter.

The dynamic model of the generalized m-level Cascaded H-Bridge converter is represented by the POG block scheme shown in Fig. 10. In this case there is an input resistance R_{in} for each H-Bridge: $\mathbf{R}_{in}=R_{in}\mathbf{I}_n$ where $n=(m-1)/2$. Vector $\mathbf{B}_n$ is a n-dimensional column vector with all its component equal to 1. Matrix $\mathbf{C}_n$ is a n-dimensional diagonal matrix with the values of the capacitors C_1, C_2, ..., C_n on its diagonal. The state space equations are the following

$$\left[\begin{array}{cccc} C_1 & 0 & \dots & 0 \\ 0 & C_2 & \dots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \dots & C_n \end{array}\right]\left[\begin{array}{c} \dot{V}_1 \\ \dot{V}_2 \\ \vdots \\ \dot{V}_n \end{array}\right]=\left[\begin{array}{cccc} -\frac{1}{R_{in}} & 0 & \dots & 0 \\ 0 & -\frac{1}{R_{in}} & \dots & 0 \\ \vdots & \vdots & \ddots & \vdots \\ 0 & 0 & \dots & -\frac{1}{R_{in}} \end{array}\right]\left[\begin{array}{c} V_1 \\ V_2 \\ \vdots \\ V_n \end{array}\right]-\left[\begin{array}{c} s_1 \\ s_2 \\ \vdots \\ s_n \end{array}\right]I_{out}+\left[\begin{array}{c} \frac{1}{R_{in}} \\ \frac{1}{R_{in}} \\ \vdots \\ \frac{1}{R_{in}} \end{array}\right]V_{dc}.$$

The vector $\mathbf{S}_n$ of the control signals s_i is the following

$$\mathbf{S}_n=[\overline{T}_2T_1-T_2\overline{T_1},\ \overline{T_4}T_3-T_4\overline{T_3},\ ...,\ \overline{T_{2n}}T_{2n-1}-T_{2n}\overline{T_{2n-1}}]^{\mathrm{T}} \quad (4)$$

in order to have $V_{out}=V_{A0}$.

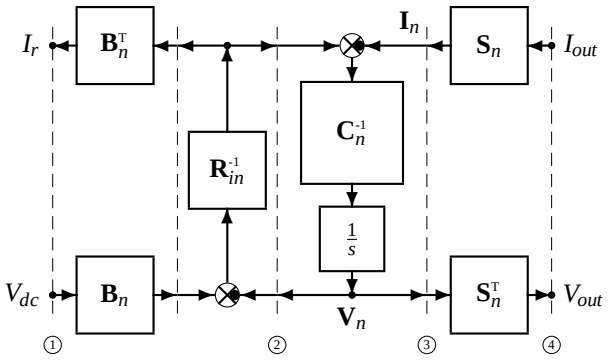

Fig. 10. POG dynamic model of a m-level cascaded H-Bridge converter: $n=(m-1)/2$.

VI. Simulation of the models

The Matlab/Simulink® block scheme used to simulate the POG model of a Cascaded H-Bridge multilevel converter is shown in Fig. 11. In particular, the multilevel converter is controlled by the control signals T_i generated by a PWM subsystem which implements different types of modulation techniques (PD, POD and APOD) for a generic number m of voltage levels. The PWM subsystem has been designed to provide the control signals T_i for all the three types of multilevel converters presented in this paper. The Cascaded H-Bridge converter considered in Fig. 11 uses relation (4) to

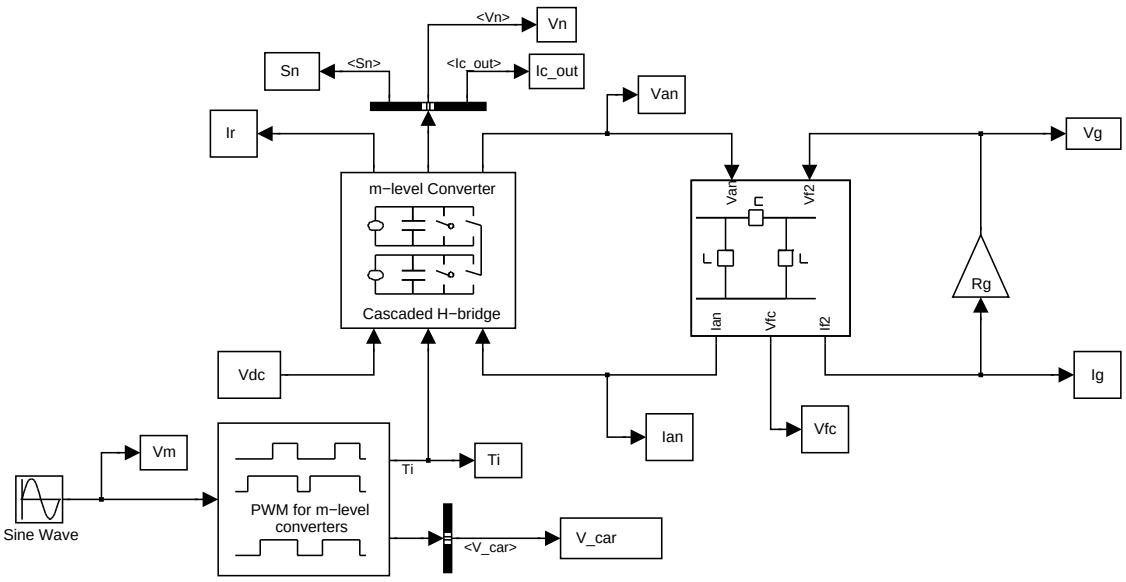

Fig. 11. Matlab-Simulink® block scheme used to simulate the POG model of a cascaded H-Bridge multilevel converter.

generate the control vector $\mathbf{S}_n$ by signals T_i. The *LCL* filter present in the simulation scheme is used to reduce the high order harmonics introduced by the PWM modulation. The parameters for the filter are the following: $C = 3\,\mu$F, $L_1 = 0.8$ mH, $L_2 = 0.4$ mH, $R_1 = 0.1\,\Omega$ and $R_2 = 0.05\,\Omega$. The POG model of the considered *LCL* filter is described in [13].

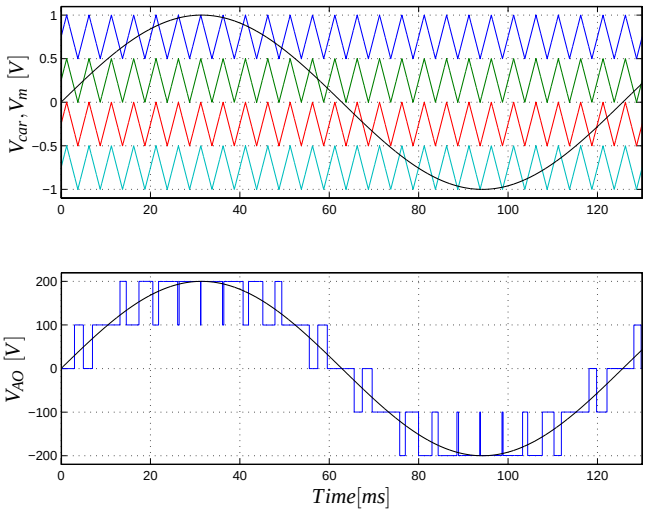

Fig. 12. Five-level Cascaded H-Bridge: PD triangular carriers V_{car}, modulation voltage V_m and output signal V_{AO}.

A. Simulation results

1) Cascaded H-Bridge converter: The considered 5-level Cascaded H-Bridge converter is characterized by the following parameters: PWM carrier frequency $f_c = 200$ Hz, modulation frequency $f_g = 50$ Hz, input voltage $V_{dc} = 100$ V, input resistance $R_{in} = 1\,\Omega$, output resistance $R_g = 50\,\Omega$ and internal capacitors $C_i = 80$ mF. The waveforms of the triangular carriers V_{car}, the modulation voltage V_m and the output voltage V_{AN}

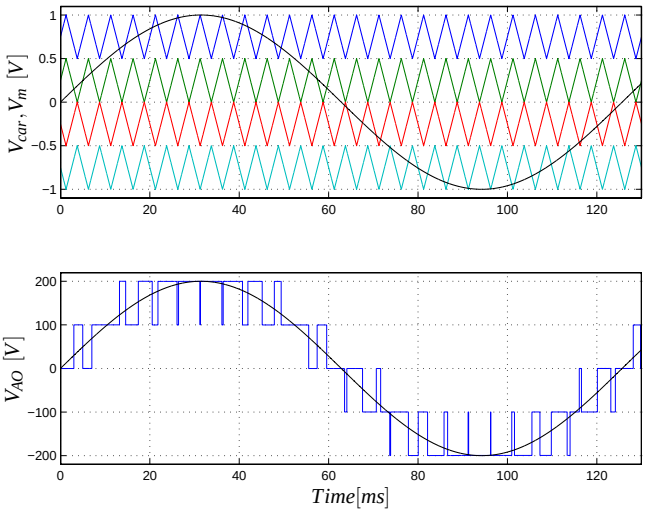

Fig. 13. Five-level Cascaded H-Bridge: POD triangular carriers V_{car}, modulation voltage V_m and output signal V_{AO}.

are shown in Fig. 12, Fig. 13 and Fig. 14, respectively for the following three different types of PWM modulation: PD, POD and APOD. Notice that in this case the frequency of the PWM carrier has been chosen quite small in order to clearly show the different behaviors obtained with the three different types of PWM modulation.

2) Diode-Clamped converter: A 5-level Diode-Clamped converter has been considered. The following parameters have been used: $V_{in} = 100$ V, PWM carrier frequency $f_c = 17$ kHz and modulation frequency $f_g = 50$ Hz. The simulation results obtained using a PD-PWM modulation and when $V_{out} = V_{AN}$ are shown in Fig. 15. Notice that in this case the considered PWM carrier frequency is high and the filtered output voltage V_g has a sinusoidal time behavior quite similar to the modulation voltage V_m.

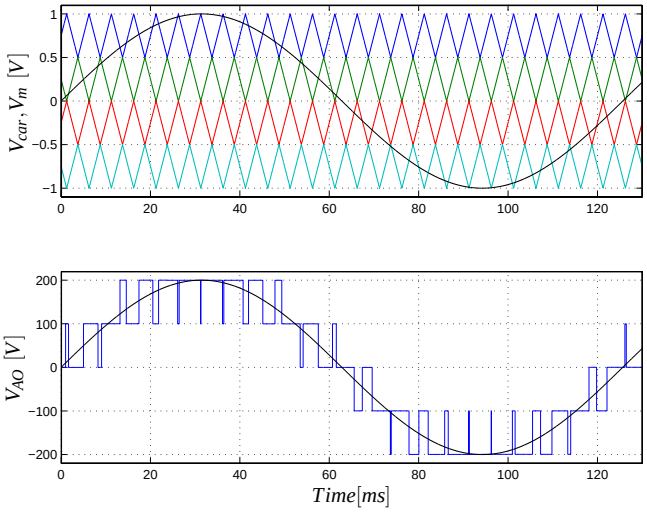

Fig. 14. Five-level Cascaded H-Bridge: APOD triangular carriers V_{car}, modulation voltage V_m and output signal V_{AO}.

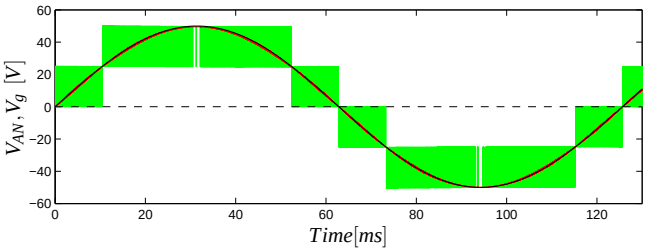

Fig. 15. Output voltage V_{AN} and filtered signal V_g of a 5-level Diode-Clamped converter obtained using a PD modulation.

3) Flying-Capacitor converter: A 5-level Flying-Capacitor converter has been considered. The following parameters have been used: $V_{in} = 100$ V, carrier frequency $f_c = 17$ kHz, modulation frequency $f_g = 50$ Hz. The simulation results obtained using a POD-PWM modulation and when $V_{out} = V_{A0}$ are shown in Fig. 16.

VII. Conclusion

In this paper the dynamic models of three different types of multilevel converters obtained using the Power Oriented Graphs technique have been presented. The simulation results confirm the validity of the proposed models. The POG dynamic models have the advantage to be easy to use, easy to understand and can be directly implemented and simulated in Matlab-Simulink® environment. Variants on the proposed POG models can be easily implemented and simulated in a very short time. For this reason the POG technique can be helpful to manufacturers to analyze and design new converter topologies.

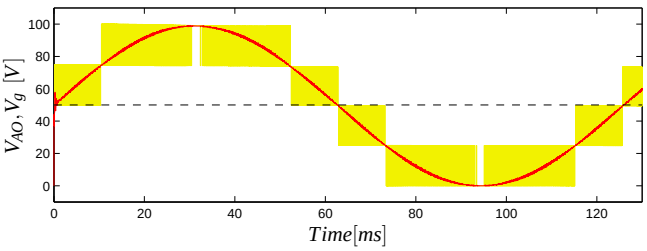

Fig. 16. Output voltage V_{AO} and filtered signal V_g of a 5-level Flying-Capacitor converter obtained using POD modulation.

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